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(54) Manufacturing process of an integrated circuit including high-density and logic components portion

(57) A process for the integration in a semiconductor chip of an integrated circuit including a high-density integrated circuit components portion and a high-performance logic integrated circuit components portion, providing for: over a semiconductor substrate (1), insulatively placing a silicidated polysilicon layer (5,11), comprising a polysilicon layer (5) selectively doped in accordance to a conductivity type of at least the high-performance logic integrated circuit components, covered by a silicide layer (11); selectively covering the silicidated polysilicon layer (5,11) with a hard mask (12); defining gate structures for the high-density integrated circuit components and for the high-performance logic integrated circuit components using said hard mask (12), the gate structures comprising the silicidated polysilicon layer (5,11) covered with the hard mask (12); in a dielectric layer (19) formed over the chip, forming contact openings for electrically contacting the high-density integrated circuit components and the high-performance logic integrated circuit components, wherein at least the contact openings for electrically contacting the high-density integrated circuit components are formed in self-alignment with the gate structures thereof.

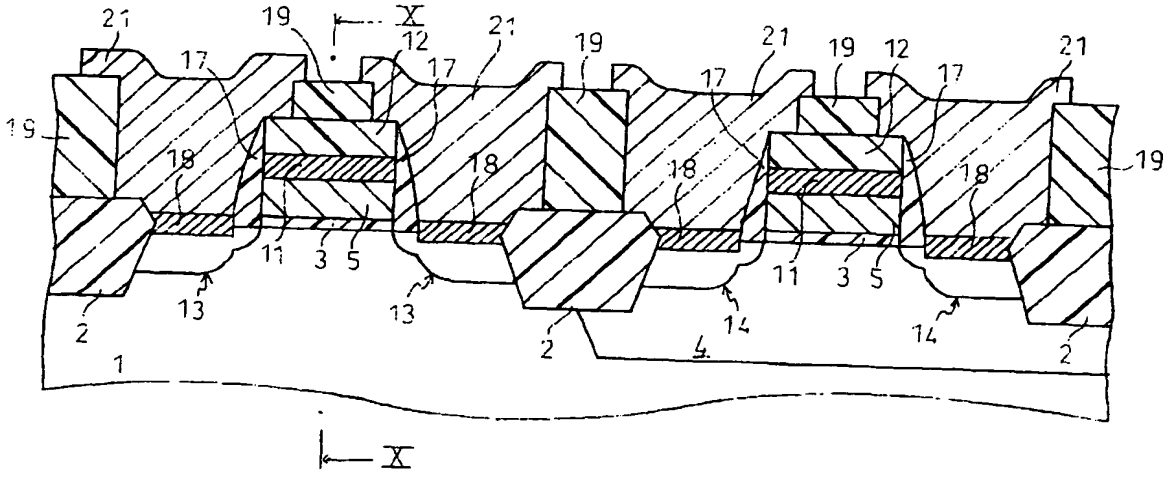

FIG.10a1

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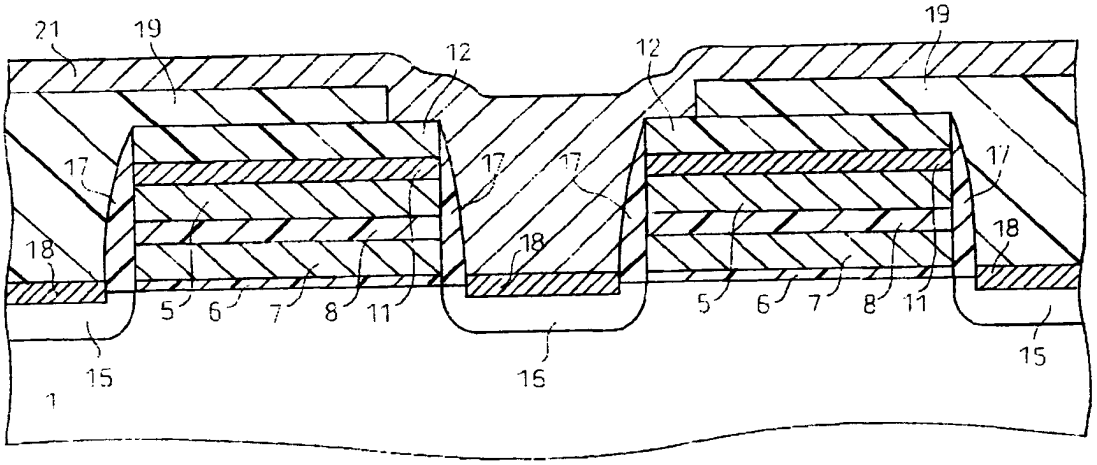


FIG . 10b

Description

[0001] The present invention relates generally to the field of integrated circuit technology, and more specifically to the manufacturing of high-density integrated circuits, typically semiconductor memories, particularly but not exclusively non-volatile ones, and logic circuits. Still more specifically, the invention relates to a manufacturing process for the integration in same chip of a high-density integrated circuit portion, typically a memory, and high-performance logic integrated circuit portion.

[0002] As known, in a semiconductor memory the most of the chip area is occupied by the array of memory cells, the so-called memory matrix. Thus, in order to keep the chip dimensions small enough while the number of memory cells increases, the dimensions of the memory cells have to be shrunk, so as to pack more and more memory cells per chip unit area.

[0003] However, one of the factors that limits the possibility of shrinking the memory cells' dimensions is the possibility of reducing the dimensions of the contacts. In a memory matrix, a large number of contacts are provided, e.g. for contacting the memory cells' drain regions by the metal bit lines. Current memory chips can have several tens of millions of contacts.

[0004] The reason why the contact dimensions cannot be easily shrunk is mainly lithographic, and gives rise to an increased defectivity, that is, a low production yield.

[0005] In recent years, several new techniques of forming contacts have been proposed, in the attempt to shrink the contact dimensions without increasing the defectivity of the memory chips. One of such new techniques is the so-called Self-Aligned Contact (shortly, SAC) technique, in which by using an anisotropic etch non-conductive layers are advantageously used to relax the contact mask design rules.

[0006] However, new difficulties now arise in view of the trend towards the integration in a same semiconductor chip of a semiconductor memory and high-performance logic circuits, for the reasons to be explained.

[0007] Conventionally, high-performance logic circuits take advantage of another technique, known as salicidation, or self-aligned silicidation, providing for a self-allgned formation of metal silicides on active areas and on polysilicon layers. The use of salicidation has made possible higher circuit performance.

[0008] Thus, the general practice now provides for using the SAC technique for the fabrication of semiconductor memories, and salicidation for the production of high-performance logic circuits.

[0009] Unfortunately, the above two techniques are scarcely compatible. This prevents or makes difficult the integration in a same chip of a memory and high-performance logic circuits.

[0010] In view of the state of the art, it has been an object of the present invention to provide a manufacturing process suitable for integrating in a same semiconductor chip a high-density integrated circuit portion and a high-performance logic integrated circuit portion.

[0011] According to the present invention, such an object has been achieved by means of a process for the integration in a semiconductor chip of an integrated circuit including a high-density integrated circuit components portion and a high-performance logic integrated circuit components portion, characterized by providing for:

over a semiconductor substrate, insulatively placing a silicidated polysilicon layer, comprising a polysilicon layer selectively doped in accordance to a conductivity type of at least the high-performance logic integrated circuit components, covered by a silicide layer;

selectively covering the silicidated polysilicon layer with a hard mask;

defining gate structures for the high-density integrated circuit components and for the high-performance logic integrated circuit components using said hard mask, the gate structures comprising the silicidated polysilicon layer covered with the hard mask; and

in a dielectric layer formed over the chip, forming contact openings for electrically contacting the high-density integrated circuit components and the high-performance logic integrated circuit components, wherein at least the contact openings for electrically contacting the high-density integrated circuit components are formed in self-alignment with the gate structures thereof.

[0012] The features and advantages of the present invention will be made clearer by the following detailed description of a possible practical embodiment thereof, illustrated merely by way of a non-limiting example in the annexed drawings, wherein:

Figures 1A, 2, 3, 4A, 5A, 6A, 7, 8A, 9A1, 9A2, 10A1 and 10A2 schematically show in cross-sectional views a sequence of the main steps of a process according to the present invention for the manufacturing of transistors of a high-performance logic circuit; and

Figures 1B and 4B to 10B schematically show in cross-sectional views a corresponding sequence of the main process steps for the manufacturing of a memory.

steps for the manufacturing of a memory.

[0013] Making reference to the drawings, Figures 1A and 1B schematically show in cross-section a first portion L and, respectively, a second portion M of a semiconductor chip in which high-performance logic circuits and a semiconductor memory will be integrated. The first portion L of the chip will host a pair of complementary transistors of a high-performance logic circuit, while

the second portion M will host a pair of memory cells of a memory cell matrix for a semiconductor memory, particularly a non-volatile memory such as an EPROM, an EEPROM or a Flash EEPROM.

[0014] Referring to Figure 1A, in a semiconductor substrate 1, for example of the P conductivity type, with suitable doping level, field oxide regions 2 are selectively formed in any conventional way, e.g. by means of the so-called LOCOS technique. Between the field oxide regions 2, a logic transistor gate oxide layer 3 is formed over a surface of the substrate 1. The thickness of the logic transistor gate oxide layer 3 is for example in the range 20-100 Å. From the logic transistor gate oxide layer 3, gate oxides of the transistors of the high-performance logic circuit will be formed.

[0015] For the formation of P-channel transistors of the high-performance logic circuit, N type wells 4 are formed in the P type substrate 1. N-channel transistors of the high-performance logic circuit can be formed directly in the P type substrate 1 or, if preferred, P type wells with suitable doping can be formed in the P type substrate 1. It is to be noted that the conductivity type of the substrate 1, and thus that of the well 4, can be opposite to those previously described.

[0016] A polysilicon layer 5 is deposited over the field oxide regions 2 and the gate oxide layer 3.

[0017] Referring now to Figure 1B, i.e. to the portion of the chip dedicated to the memory matrix, over the substrate 1 a memory cell gate oxide layer 6 is formed. From the memory cell oxide layer 6 gate oxides for the memory cells will be obtained. The oxide layer 6 can be the logic transistor gate oxide layer 3 or a different oxide layer, depending on the type of memory cells which are to be formed (EPROM, EEPROM, Flash EEPROM). The thickness of the memory cell gate oxide layer 6 is for example in the range 70-120 Å.

[0018] Over the memory cell gate oxide layer 6 a polysilicon layer 7 is deposited. The polysilicon layer 7 is a first, lower polysilicon layer (first poly), while the polysilicon layer 5 previously mentioned is a second, upper polysilicon layer (second poly) . The first polysilicon layer 7 will be used to form floating gates of the memory cells. Over the first polysilicon layer 7, a dielectric layer 8 (interpoly dielectric) is formed. Typically, the interpoly dielectric is formed as a triple layer comprised of a lower oxide layer, an intermediate nitride layer, and an upper oxide layer (Oxide-Nitride-Oxide or ONO).

[0019] The second polysilicon layer 5, which in the portion L of the chip is deposited directly over the logic transistor gate oxide layer 3, is here deposited over the interpoly dielectric layer 8. The second polysilicon layer 5 will form the control gates of the memory cells.

[0020] The process steps necessary to form the structures depicted in Figures 1A and 1B can be completely conventional, and for this reason will not be described in further detail. Starting from these structures, the second polysilicon layer 5 is then submitted to selective doping to reduce the resistivity thereof. Preferably, at least as far as the transistors of the high-performance logic circuit are concerned, the portions of the polysilicon layer 5 which will have to form the gates of N-channel transistors are doped with N type dopants, while the portions of the polysilicon layer 5 that will have to form the gates of the P-channel transistors are doped with P type dopants. To this end, two distinct masks are used: a first mask, indicated as 9 in Figure 2, is used to expose the portions of the polysilicon layer 5 that, after definition, will form the gates of N-channel transistors of the high-performance logic circuit, protecting from dopant implantation at least the portions of polysilicon layer 5 which will form the gates of the P-channel transistors of the high-performance logic circuit; the same mask 9 can also leave exposed the portions of the polysilicon layer 5 which will form the control gates of the memory cells. A suitable N type dopant, such as As or P in a dose of $5*10^{14}$ to $5*10^{15}$, is then implanted into the exposed portions of the polysilicon layer 5, that is the portions from which the gates of the N-channel transistors of the high-performance logic circuit will be formed, and optionally the portions from which the control gates of the memory cells will be formed.

[0021] Then, the first mask 9 is removed, and a second mask, indicated as 10 in Figure 3, is applied to expose the portions of the polysilicon layer 5 that, after definition, will form the gates of the P-channel transistors of the high-performance logic circuit, protecting the remaining portions of the polysilicon layer 5 (that is, the portions of the polysilicon layer 5 previously doped, and those which will form the control gates of the memory cells). A suitable P type dopant, such as B or BF_2 in a dose of $5*10^{14}$ to $5*10^{15}$, is then implanted into the exposed portions of the polysilicon layer 5. Then, also the second mask 10 is removed.

[0022] Referring now to Figures 4A and 4B, a metal silicide layer 11, e.g. WSi_2, is then formed over the polysilicon layer 5 to further increase the conductivity thereof. To this end, a layer of a suitable metal, such as W, is first deposited over the polysilicon layer 5; then, by means of a suitable thermal treatment, the metal atoms are made to react with the silicon atoms in the polysilicon layer 5 so as to form the silicide layer 11. The silicide layer 11, also called polycide, is formed over the whole of the polysilicon layer 5, that is both over the portions of the polysilicon layer 5 that will form the gates of the N-channel and P-channel transistors of the high-performance logic circuit (Figure 4A), and over the portions of the polysilicon layer 5 which will form the control gates of the memory cells (Figure 4B). It is worth remarking that the polysilicon layer 5 is silicidated before the patterning thereof.

[0023] Then, referring to Figures 5A and 5B, a dielectric layer 12 such as a nitride layer is formed over the silicide layer 11, typically by deposition. Such a dielectric layer 12 will be used to form a so-called hard mask for the definition (patterning) of the polysilicon layer 5. Provision of a hard mask is advantageous in the definition

of sub-micrometric geometries in polysilicon layers, thanks to the fact that it increases the degree of reflectivity of the structure to be defined. After deposition of the dielectric layer 12, a photoresist layer is deposited over the chip, then by means of a photolithographic mask the photoresist layer is selectively exposed to light, it is developed to selectively remove it, and then a selective etch is carried out. By means of the etching process, the dielectric layer 12 is selectively removed, thus forming a hard mask that leaves exposed the portions of the polysilicon layer 5 which will have to be removed in the following steps.

[0024] Then, using the remaining dielectric layer 12 as a hard mask, another selective etch is carried out, to define by selective removal the polysilicon layer 5, together with the silicide layer 11, as well as the underlying layers such as, in the high-performance logic circuit region, the logic transistor gate oxide layer 3, and in the memory matrix region the interpoly dielectric 8. A following masking step will allow the etching of the first polysilicon layer 7 and the memory cell gate oxide layer 6. At the end of this etch, conventional implants are performed in order to form memory cell source and drain regions 15, 16. In this way, the gate structures shown in Figures 6A and 6B are obtained.

[0025] At this point it is possible to selectively remove the dielectric layer 12 from over the polysilicon layer 5 where it is desired to provide contacts to the polysilicon layer 5. For example, as shown in Figure 7 which is a view in cross-section of the N-channel transistor of the high-performance logic circuit along line VII-VII in Figure 6A, a resist mask 120 covers all the chip surface, except from regions of the dielectric layer 12 which are to be removed to allow access to the underlying polysilicon layer 5; preferably, such regions are located over the field oxide 2. The dielectric layer 12 is then etched away from the exposed regions, so as to expose the surface of the polysilicon layer 5.

[0026] The following process steps provide for the formation, in conventional ways, of source regions and drain regions 13 and 14 for the N-channel and, respectively, P-channel transistors of the high-performance logic circuit. The source and drain regions 13 and 14 of the transistors of the high-performance logic circuit have the so-called Lightly-Doped Drain (LDD) structure, with a shallower, relatively lightly doped portion 131, 141 aside the gate structures, and a deeper, more heavily doped portion 132, 142 farther from the gate structures. Such a structure is obtained by firstly introducing into the substrate, in self alignment with the gate structures of the transistors, a relatively light dose of dopants, then forming insulating material sidewall spacers 17 at the sides of the gate structures, extending down to the substrate surface so as to cover the lightly doped portions 131, 141 of the source and drain regions 13, 14, and then forming the deeper, more heavily doped portions 132, 142 of the source and drain regions. Sidewall spacers 17 are also inherently formed at the sides of the gate structures of the memory cells.

[0027] Salicidation of the active areas is also contemplated:

to this end, a layer of a suitable metal such as Ti or Co is firstly deposited over the whole surface of the chip, then a thermal treatment is carried out; during the thermal treatment, the metal atoms react with silicon atoms to form a metal silicide; this only takes place where the metal atoms lies directly over silicon or polysilicon, while over the dielectric layers and the sidewall spacers no reaction takes place and no silicide is formed. At the end of the thermal treatment, the unreacted metal atoms are removed:

self-aligned metal silicide, or salicide, regions 18 are thus formed over the deeper, more heavily doped portions 132, 142 of the source and drain regions 13, 14 of the transistors, and over the source and drain regions 15, 16 of the memory cells (Figures 8A and 8B). It is to be noted that salicide regions 18 are not formed over the polysilicon layer 5, since the latter is covered by the dielectric hard mask 12, except where the polysilicon layer 5 is not covered by the dielectric layer 12, i.e. where contacts to the polysilicon layer 5 (Figure 9A2). The fact that the polysilicon layer 5 is not salicidated is not a problem, and does not affect the performance of the logic circuit. In fact, according to the present invention, the polysilicon layer 5 has previously been submitted to a blank silicidation and a polycide layer 11 has been formed over the polysilicon layer 5. The electric performance of the polycide layer 11 are substantially equivalent to those of a salicide layer. In addition, the formation of salicide regions 18 where contacts to the polysilicon layer 5 are to be formed improves the contact conductivity.

[0028] After these steps, referring to Figures 9A1, 9A2 (which is a cross-section along line IX-IX in Figure 9A1) and 9B, the structure is ready to receive by deposition a dielectric layer 19, in which contact openings will formed. In order to define contact openings, a mask 20 (contact mask) is applied to the dielectric layer 19, the mask 20 leaving exposed the portions of the dielectric layer 19 that will have to be removed so as to open contact openings. It is to be noted that the openings in the contact mask 20 extend over the gate structures of the memory cells, and possibly also over the gate structures of the transistors of the high-performance logic circuit. In other words, the contact openings to be opened in the dielectric layer are defined in self-alignment with the gate structures of the memory cells and, possibly, also of the transistors of the high-performance logic circuit. However, this is not a concern, since during the following selective etch to remove the dielectric layer 19, such gate structures are not damaged, due to the presence of the hard mask layer 12 and the sidewall spacers 17 that protect the polysilicon layer 5.

[0029] Referring to Figures 10A1, 10A2 (which is a cross-section along line X-X in Figure 10A1) and 10B, after having defined contact openings in the dielectric

layer 19, a metal layer 21 is deposited over the chip; the metal layer 21 penetrates into the contact openings thus contacting, through the respective salicide regions 18, the source and drain regions 13, 14 and the gate of the transistors of the high performance logic circuit, and the drain regions 16 of the memory cells. Similar contacts to the source regions 15 of the memory cells, not shown, will clearly be provided for in selected regions of the memory matrix. The metal layer 21 is then patterned to define metal strips.

[0030] The process according to the present invention is suitable for the integration in a same chip of a high-performance logic circuit and a memory, particularly a non-volatile one.

[0031] The process according to the invention allows to take advantage of the techniques of salicidation of active areas, from one hand, and Self-Aligned Contact (SAC) formation from the other hand: the first technique allows to increase the performance of logic circuits, by reducing the resistivity of the source and drain regions of the transistors, while the second technique allows to form compact arrays of a memory cells.

[0032] The process according to the present invention allows to adopt the SAC technique without for this reason preventing the possibility of forming highly conductive, properly doped gate structures for the transistors of the high-performance logic circuit and the memory cells. This result is achieved by submitting the polysilicon layer from which the gates of the transistors, and the control gates of the memory cells are formed to a proper doping to achieve the correct work function, and to a blank silicidation before the definition of the gate structures. The silicidated polysilicon layer is then protected by a hard mask, which will protect the gate structures during formation of contact openings; in this way, it is possible to have contact openings extending over the gate structures of the memory cells without the risk of damaging the gate structures themselves.

[0033] It is to be noted that the steps of properly doping, with N type and P type dopants, the polysilicon layer 5, not necessarily have to be performed before silicidation thereof; as an alternative, the polysilicon layer 5 can be submitted to the required doping even after the blank formation of the silicide layer 6.

[0034] Even if not explicitly shown in the previous description, the process according to the present invention allows to integrate, together with a memory and high-performance logic circuits, transistors capable of handling a relatively high voltage, higher than the operating voltage of the high performance logic circuits. Such transistors, called H(igh) V(oltage) transistors, could be necessary for the memory, for example in order to perform electrical modification of the content thereof. HV transistors can have a structure similar to that of the transistors of the high performance logic circuits, except for a thicker gate oxide.

[0035] While the invention has been particularly shown and described with reference to a preferred embodiment thereof, it will be understood by those skilled in the art that various changes in form and details may be made without departing from the scope of the invention, defined in the appended claims.

[0036] For example, the specific gate structure of the memory cells is unessential, depending solely on the specific kind of memory to be integrated. A memory with single polysilicon level memory cells can for example be fabricated using the process of the invention.

[0037] The process according to the present invention is equally not limited to the integration of non-volatile memories, being more generally suitable for the integration of any kind of semiconductor memory.

[0038] Still more generally, the process according to the invention is suitable for the integration in a semiconductor chip of an integrated circuit including a high-density integrated circuit components portion and a high-performance logic integrated circuit components portion.

Claims

1. Process for the integration in a semiconductor chip of an integrated circuit including a high-density integrated circuit components portion and a high-performance logic integrated circuit components portion, **characterized by** providing for:

   over a semiconductor substrate (1), insulatively placing a silicidated polysilicon layer (5,11), comprising a polysilicon layer (5) selectively doped in accordance to a conductivity type of at least the high-performance logic integrated circuit components, covered by a silicide layer (11) ;
   selectively covering the silicidated polysilicon layer (5,11) with a hard mask (12);
   defining gate structures for the high-density integrated circuit components and for the high-performance logic integrated circuit components using said hard mask (12), the gate structures comprising the silicidated polysilicon layer (5,11) covered with the hard mask (12); and
   in a dielectric layer (19) formed over the chip, forming contact openings for electrically contacting the high-density integrated circuit components and the high-performance logic integrated circuit components, wherein at least the contact openings for electrically contacting the high-density integrated circuit components are formed in self-alignment with the gate structures thereof.

2. Process according to Claim 1, for the integration in a same semiconductor chip of a memory and high-performance logic circuits, **characterized by** providing for:

over a semiconductor substrate (1), insulatively placing a polysilicon layer (5) to be used to form gate structures of memory cells of the memory and of transistors of the high-performance logic circuits;
selectively doping first portions of the polysilicon layer (5), from which gate structures for N-channel transistors of the high-performance logic circuits will be obtained, with N type dopants;
selectively doping second portions of the polysilicon layer (5), from which gate structures for P-channel transistors of the high-performance logic circuits will be obtained, with P type dopants;
silicidating (11) the polysilicon layer (5) to obtain a silicidated polysilicon layer (5,11);
selectively covering the silicidated polysilicon layer (5,11) with a hard mask (12);
defining gate structures for the memory cells and for the transistors of the high-performance logic circuits using said hard mask (12), the gate structures comprising the silicidated polysilicon layer (5,11) covered with the hard mask (12);
forming source and drain regions (13-16) for the memory cells and for the transistors of the high-performance logic circuits;
forming insulating material sidewall spacers (17) aside said gate structures;
salicidating (18) at least the source and drain regions (13,14) of the transistors of the high-performance logic circuits;
forming a dielectric layer (19) over the chip;
forming contact openings in the dielectric layer (19) for electrically contacting the memory cells and the transistors of the high-performance logic circuits, at least the contact openings for electrically contacting the memory cells extending over the gate structures of the memory cells.

3. Process according to Claim 2, in which said silicidating (11) the polysilicon layer (5) provides for depositing metal atoms over the whole polysilicon layer (5), and submitting the chip to a thermal treatment to make the metal atoms react with the silicon atoms of the polysilicon layer (5), so as to obtain a metal silicide layer (11) covering the whole polysilicon layer (5).

4. The process according to Claim 3, in which said metal atoms are atoms of W.

5. Process according to Claim 2, 3 or 4, in which said steps of selectively doping the first portions and the second portions of the polysilicon layer (5) are performed before said step of silicidating the polysilicon layer (5).

6. Process according to Claim 2, 3 or 4, in which said steps of selectively doping the first portions and the second portions of the polysilicon layer (5) are performed after said step of silicidating the polysilicon layer (5), but before said step of selectively covering the silicidated polysilicon layer (5,11) with the hard mask (12).

7. Process according to Claim 5 or 6, in which said selectively covering the silicidated polysilicon layer (5,11) with a hard mask (12) provides for covering the silicidated polysilicon layer (5,11) with a nitride layer (12), and selectively removing the nitride layer (12).

8. Process according to anyone of Claims 1 to 7, in which also the source and drain regions (15,16) of the memory cells are salicidated.

9. Process according to Claim 8, in which said forming source and drain regions (13,14) for the transistors of the high-performance logic circuits provides for forming first source and drain region portions (131,141) aside the gate structures of the transistors of the high-performance logic circuits, and second source and drain region portions (132,142) farther from the gate structures, the first source and drain region portions being lightly doped and shallow compared to the second source and drain region portions.

10. Process according to Claim 9, in which the sidewall spacers (17) cover the first source and drain region portions (131,141).

11. Process according to Claim 10, in which said salicidation of the source and drain regions (13-16) is, for the transistors of the high-performance logic circuits, a salicidation of the second source and drain region portions (132,142).

12. Process according to Claim 11, in which said salicidation of the source and drain regions (13-16) provides for depositing a layer of metal atoms, and submitting the chip to a thermal treatment, so that where the layer of metal atoms overlies the source and drain regions (13-16) the metal atoms react with the semiconductor atoms to form salicide regions (18), and then removing the unreacted layer of metal atoms from the chip.

13. Process according to anyone of Claims 2 to 12, in which also the contact openings for electrically contacting the transistors of the high-performance logic circuits extend over the gate structures of the transistors.

14. Process according to anyone of Claims 2 to 13, in which in order to electrically contact the silicidated polysilicon layer (5,11) the hard mask layer (12) is selectively removed from over the silicidated polysilicon layer (5,11) where electrical contacts thereto are to be formed, before the forming of the dielectric layer (19), and then contact openings are formed in the dielectric layer (19) for electrically contacting the silicidated polysilicon layer (5,11).

15. Process according to Claim 13, in which electrical contacts to the silicidated polysilicon layer (5,11) are formed in regions of the chip where the silicidated polysilicon layer (5,11) lies over thick oxide regions (2).

16. An integrated circuit comprising, integrated in a same semiconductor chip, a high-density integrated circuit components portion and a high-performance logic integrated circuit components portion, **characterized in that** gate structures for the high-density integrated circuit components and for the high-performance logic integrated circuit components include a silicidated polysilicon layer (5,11) comprising a polysilicon layer (5), selectively doped in accordance to a conductivity type of at least the high-performance logic integrated circuit components, covered by a silicide layer (11), protected by a hard mask (12), and contact openings in a dielectric layer (19) for electrically contacting the high-density integrated circuit components and the high-performance logic integrated circuit components, wherein at least the contact openings for components, wherein at least the contact openings for electrically contacting the high-density integrated circuit components are self-aligned with the gate structures thereof.

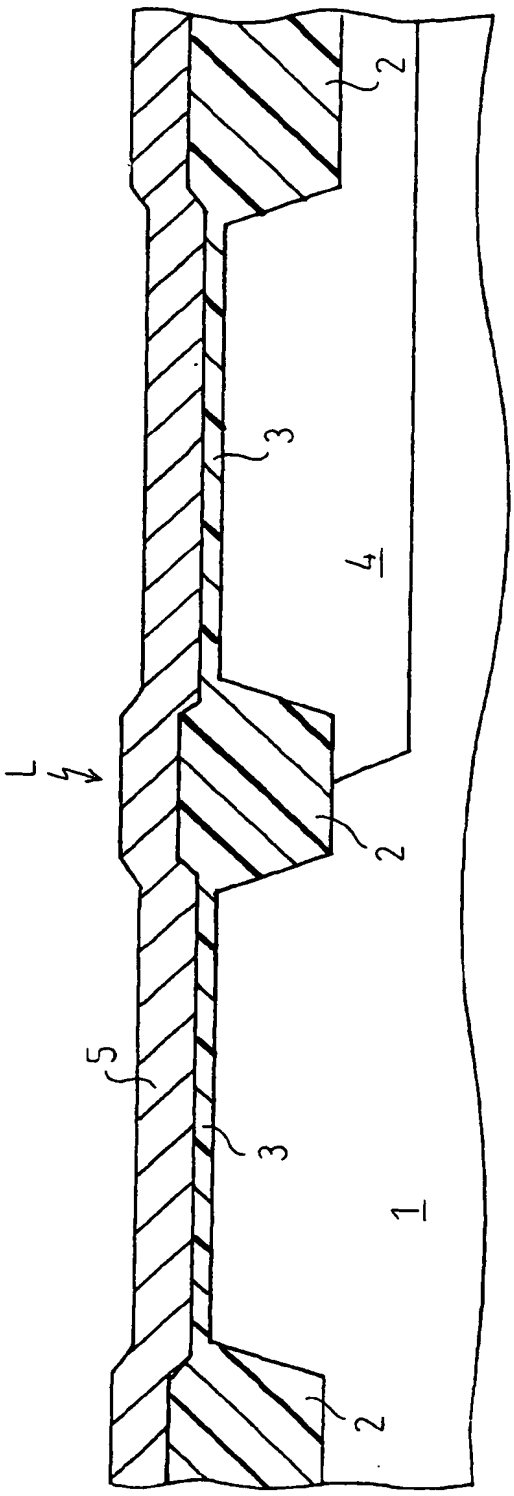


FIG. 1a

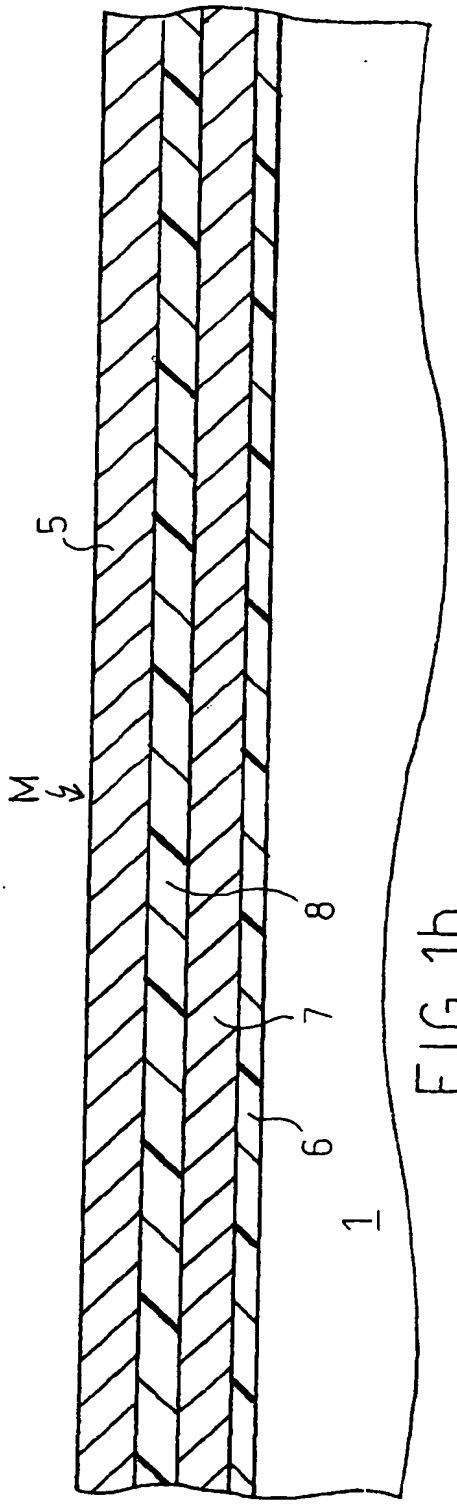


FIG. 1b

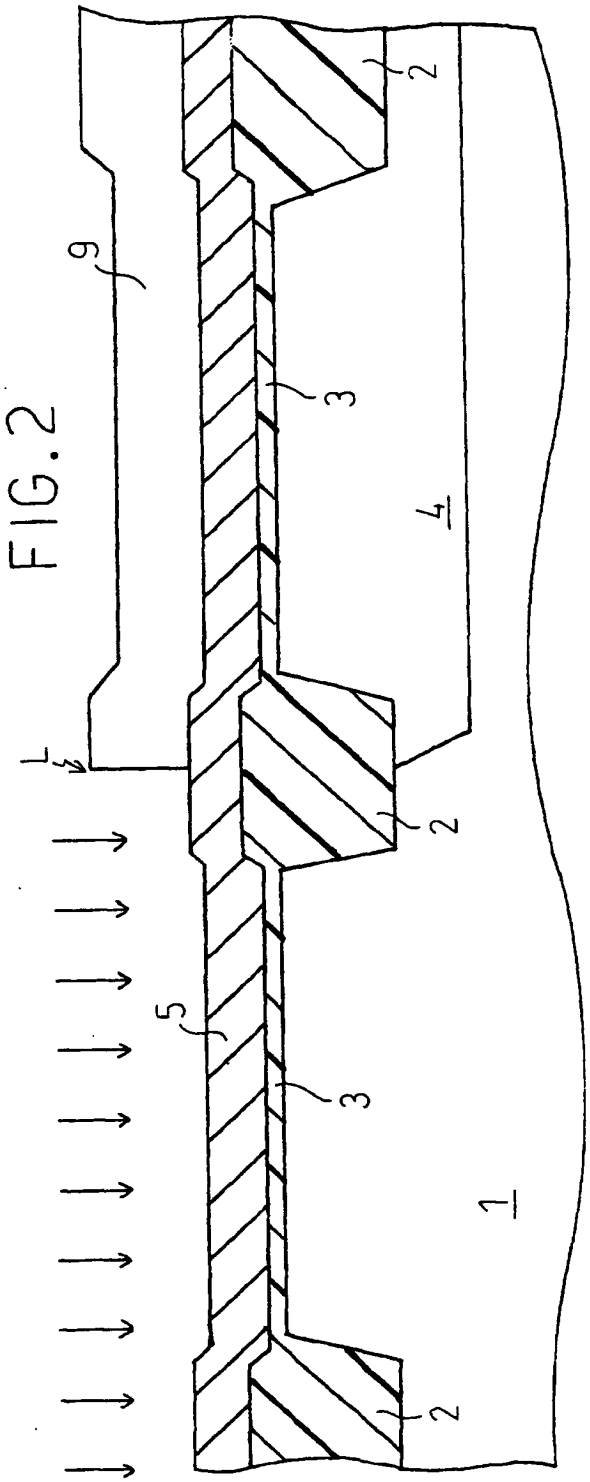


FIG.2

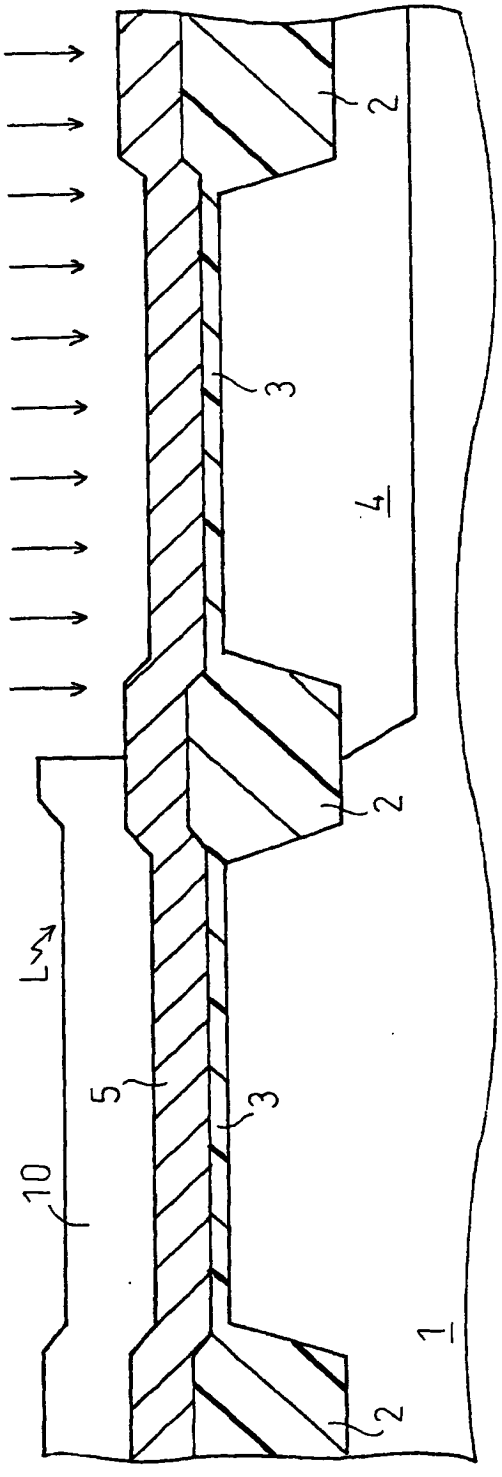


FIG.3

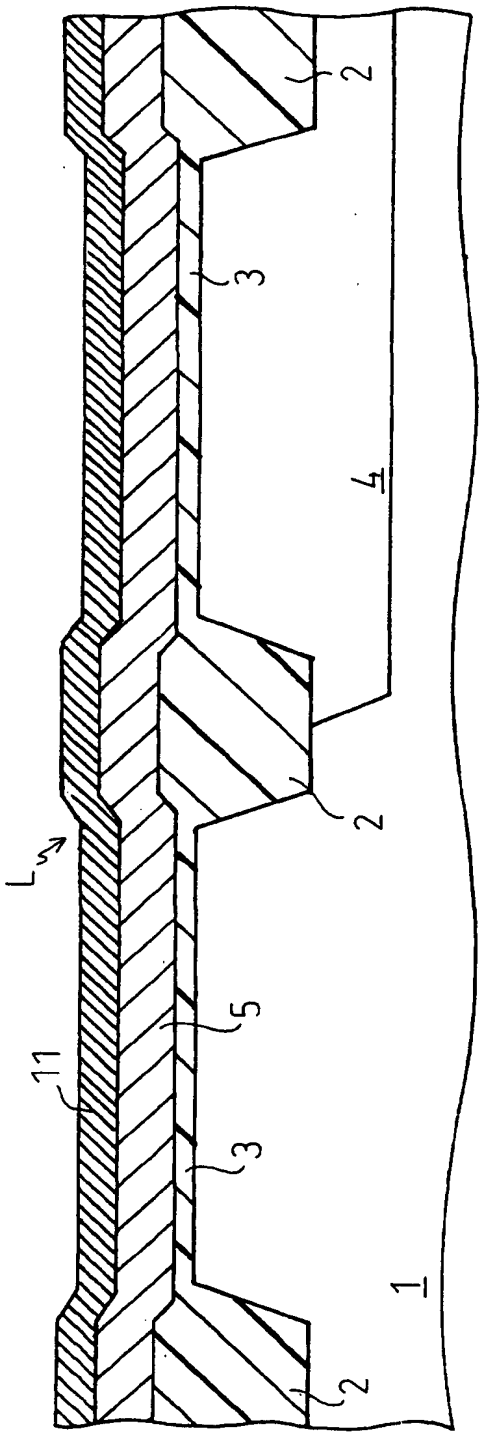


FIG. 4a

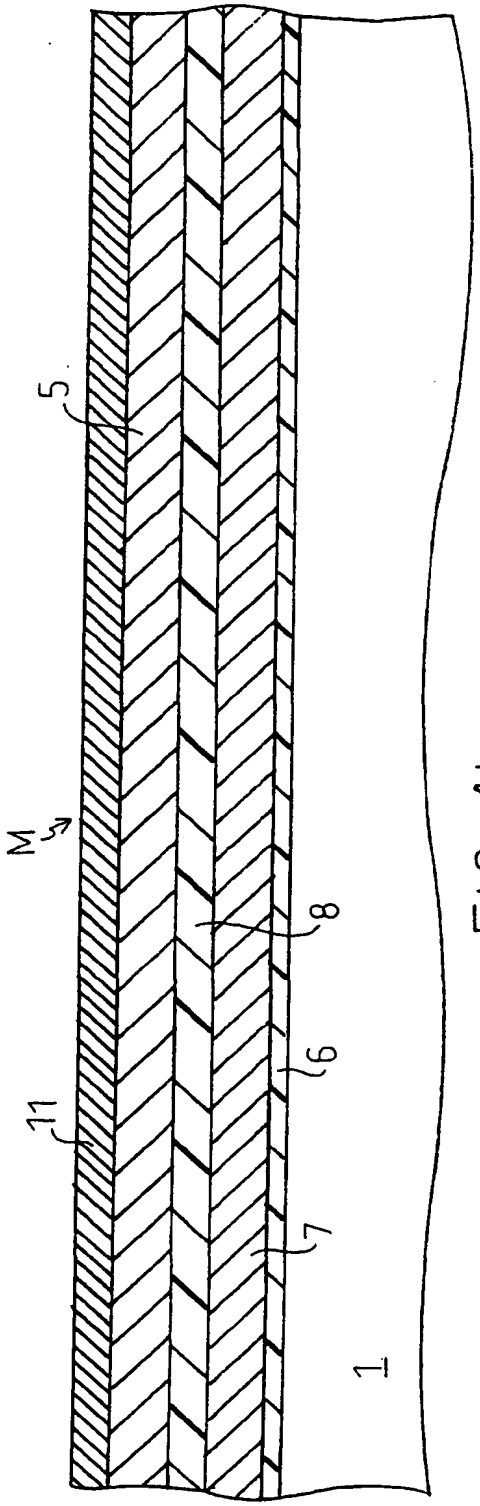


FIG. 4b

FIG. 5a

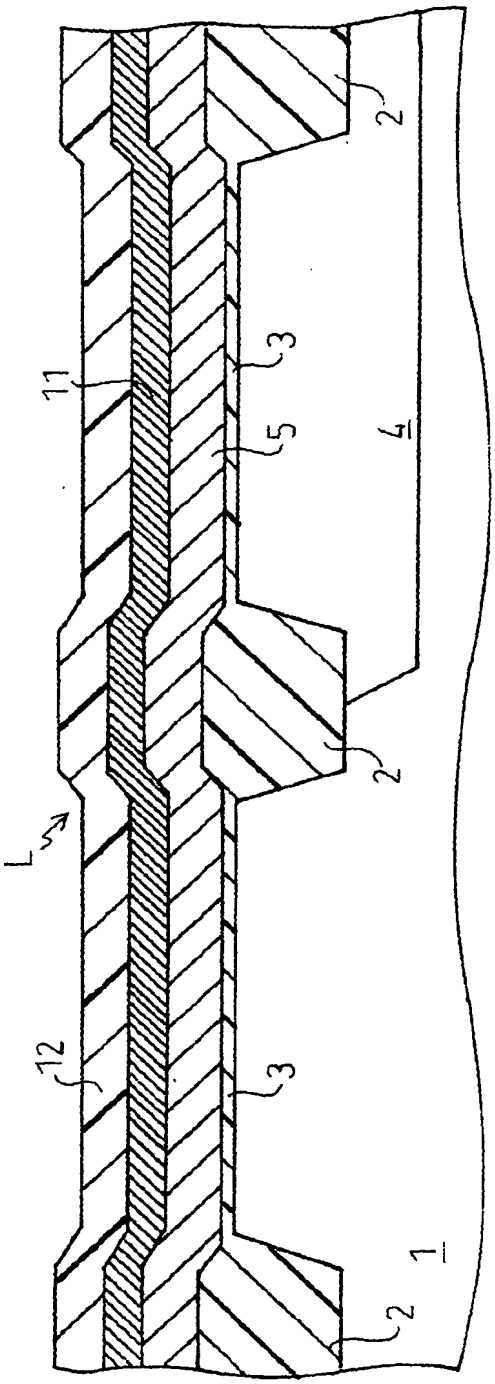


FIG.5b

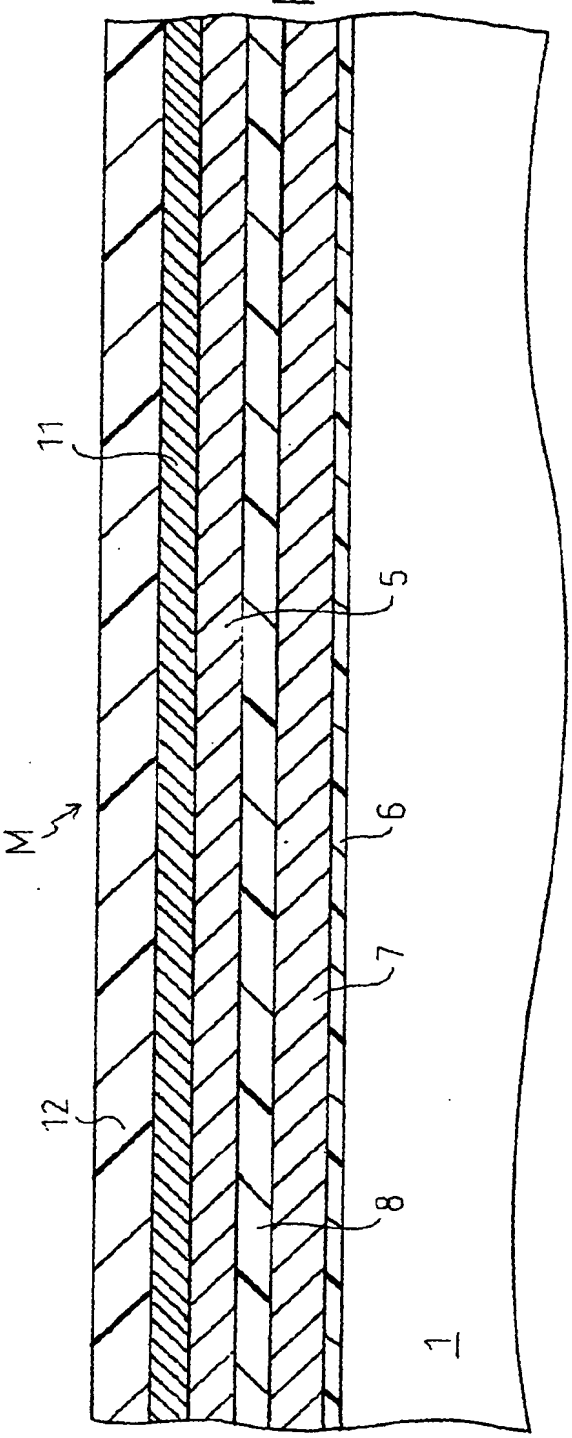


FIG. 6a

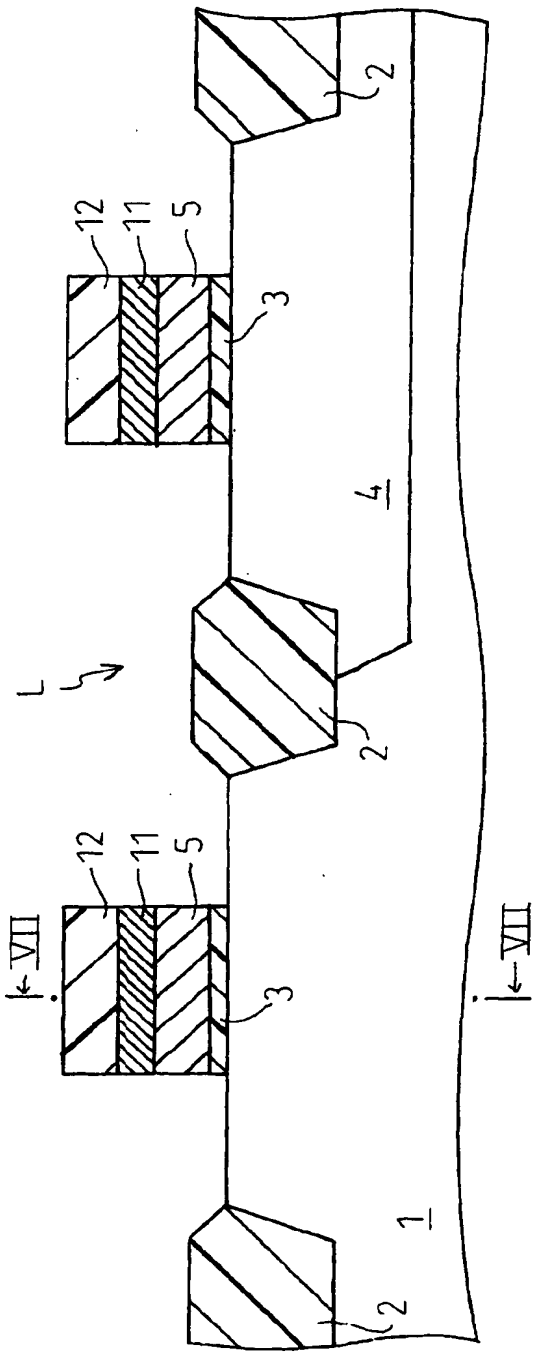
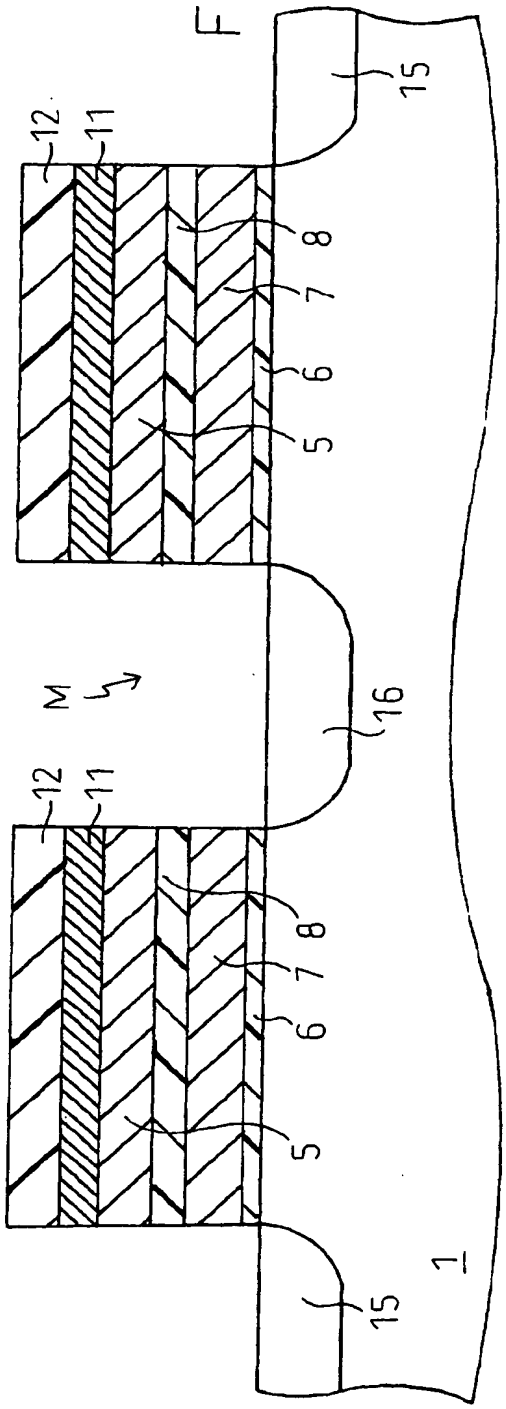


FIG. 6b



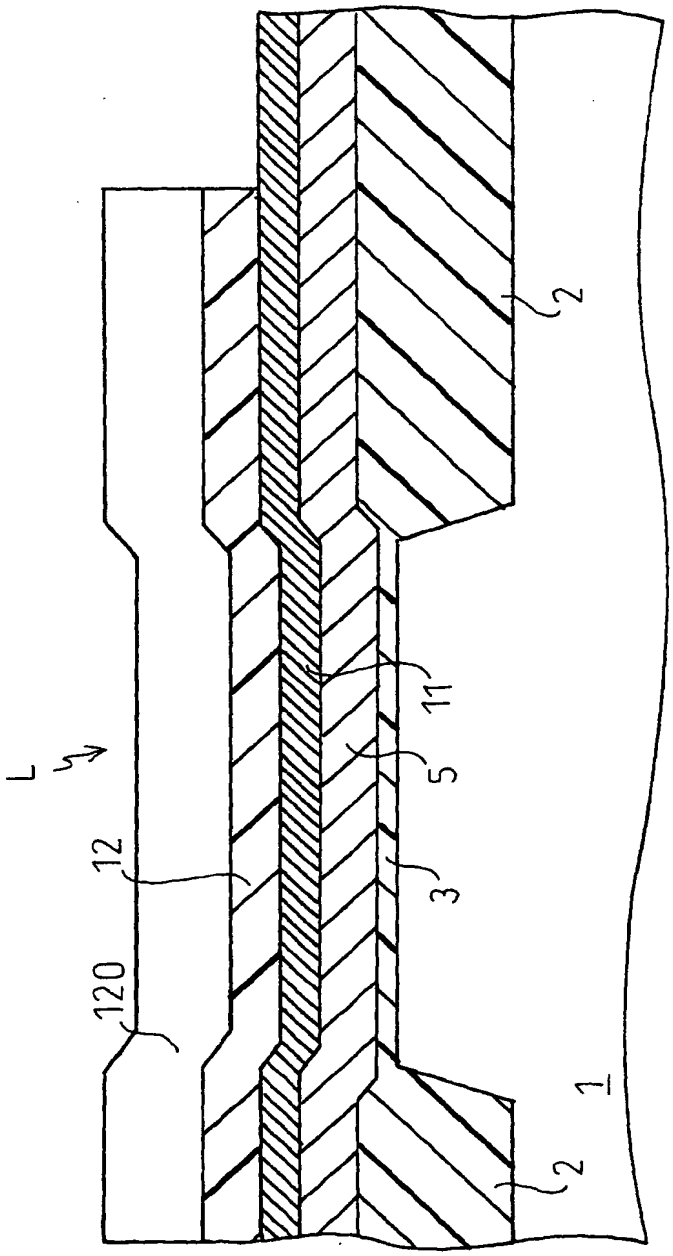


FIG.7

FIG. 8a

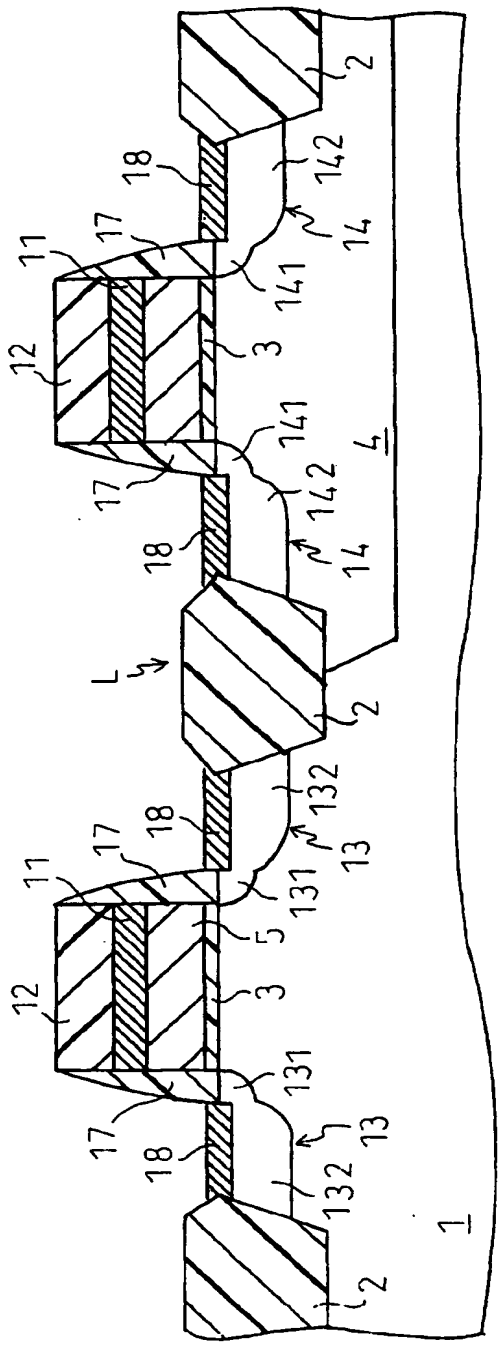
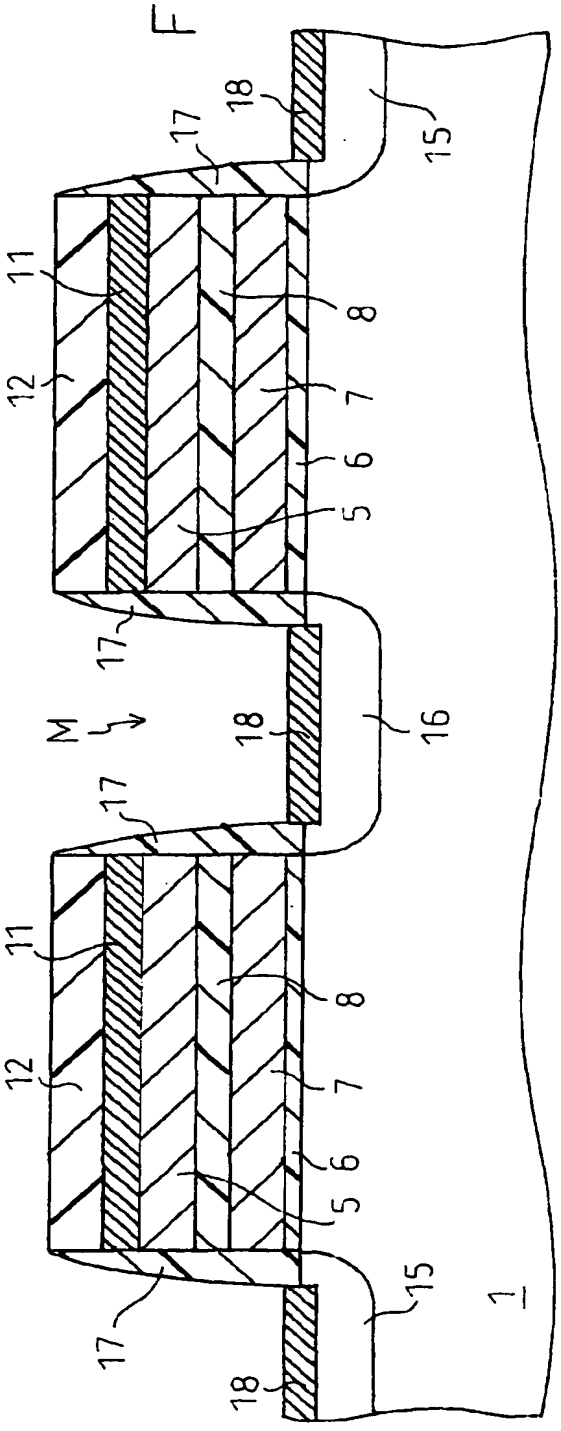


FIG. 8b



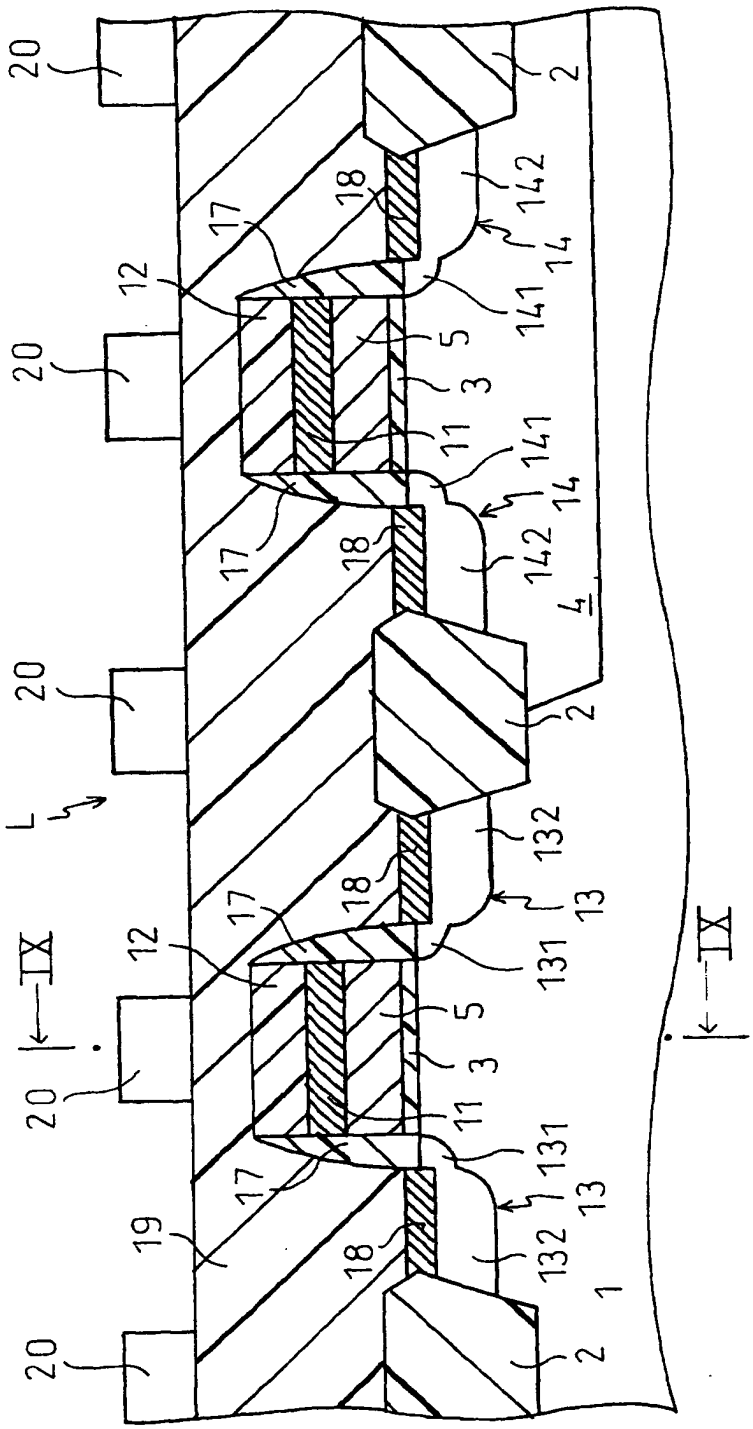


FIG. 9a1

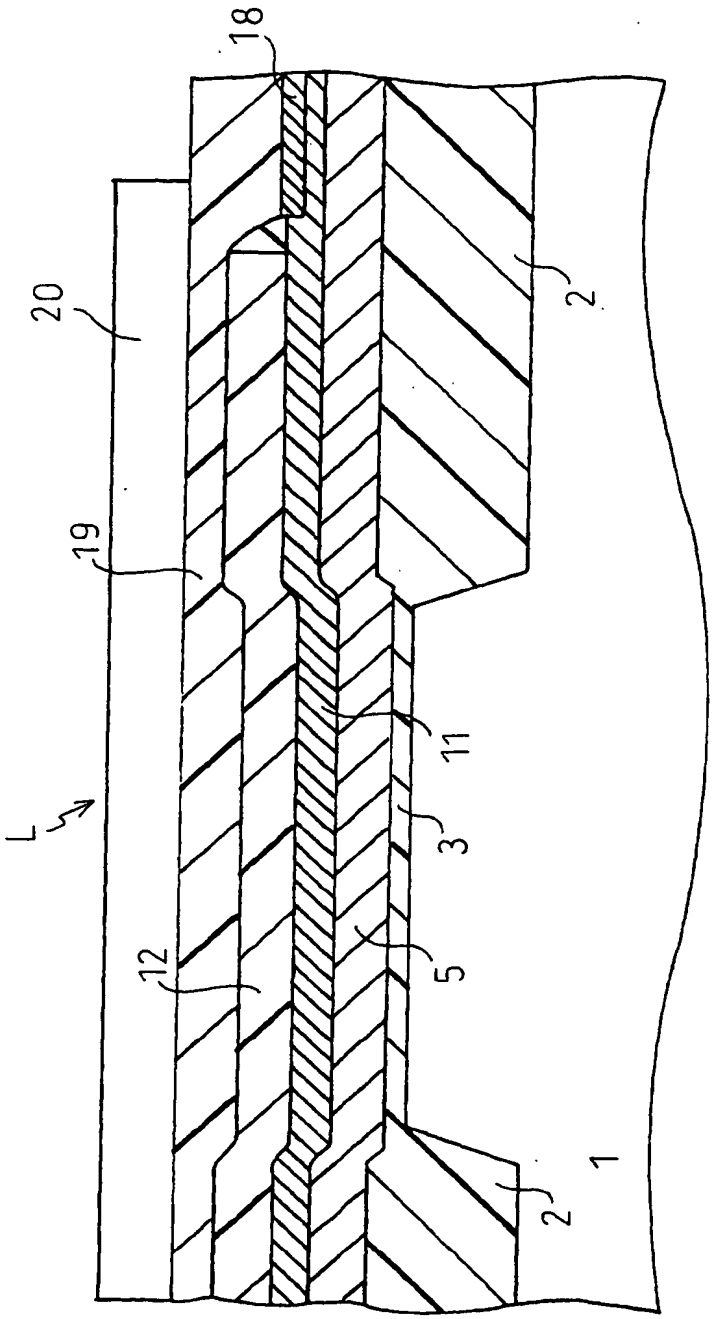


FIG. 9a2

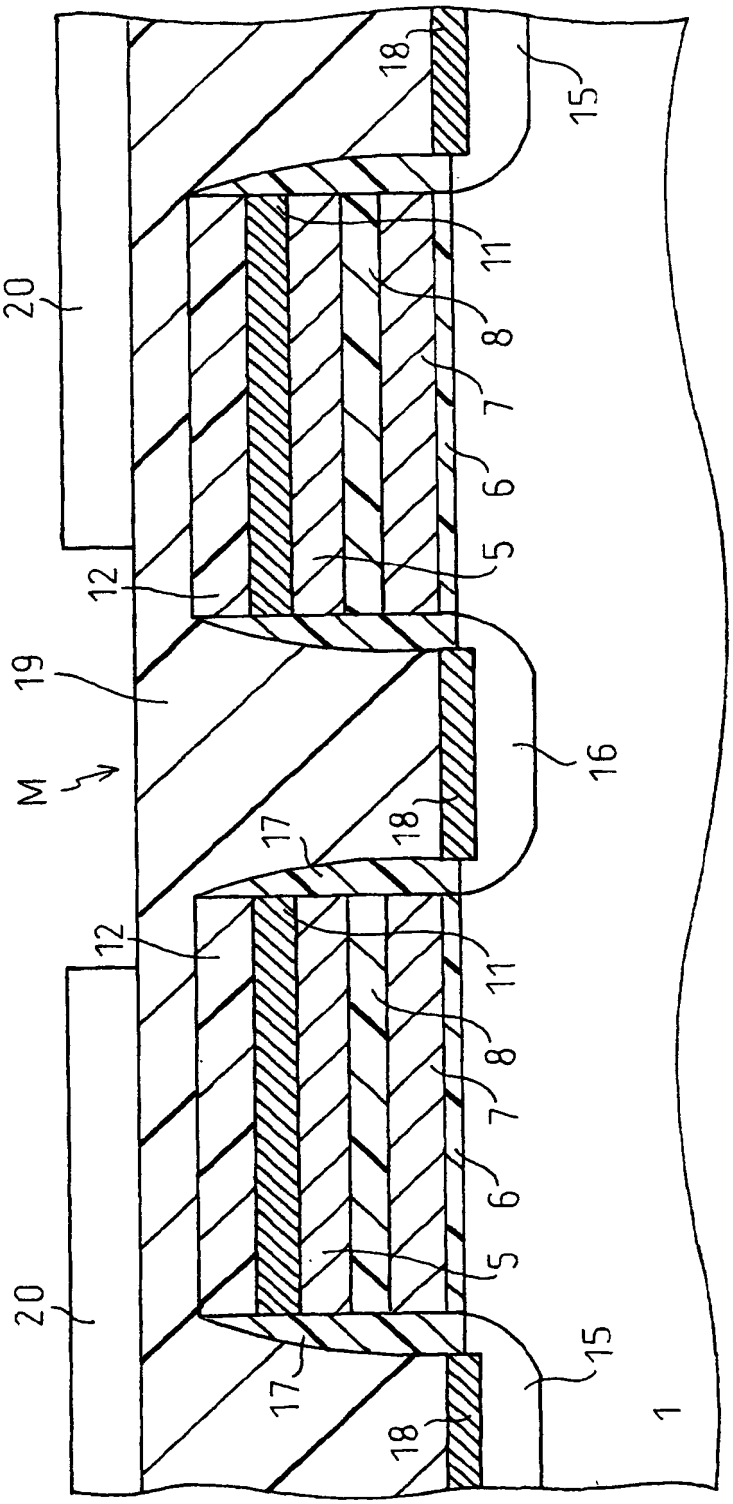


FIG. 9b

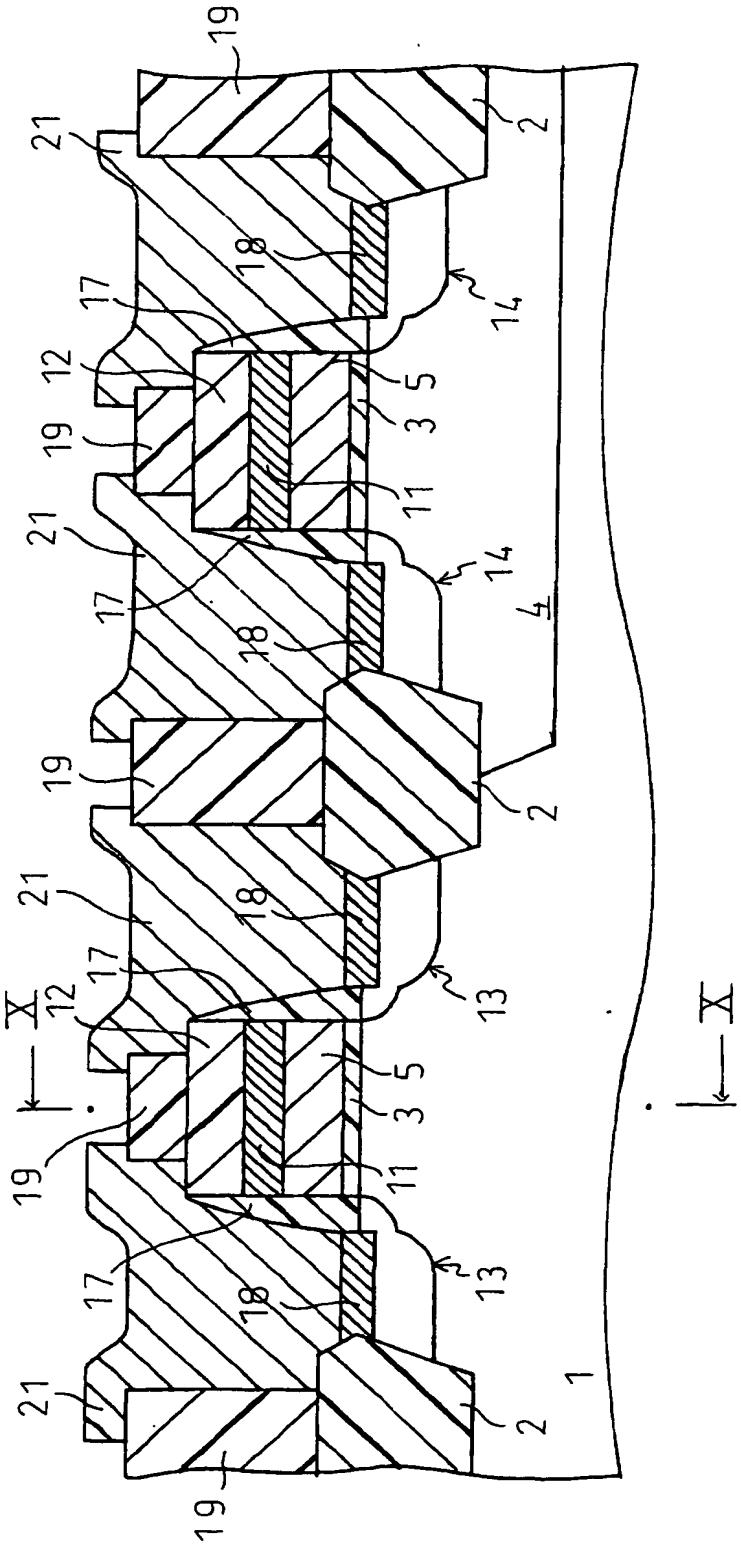


FIG.10a1

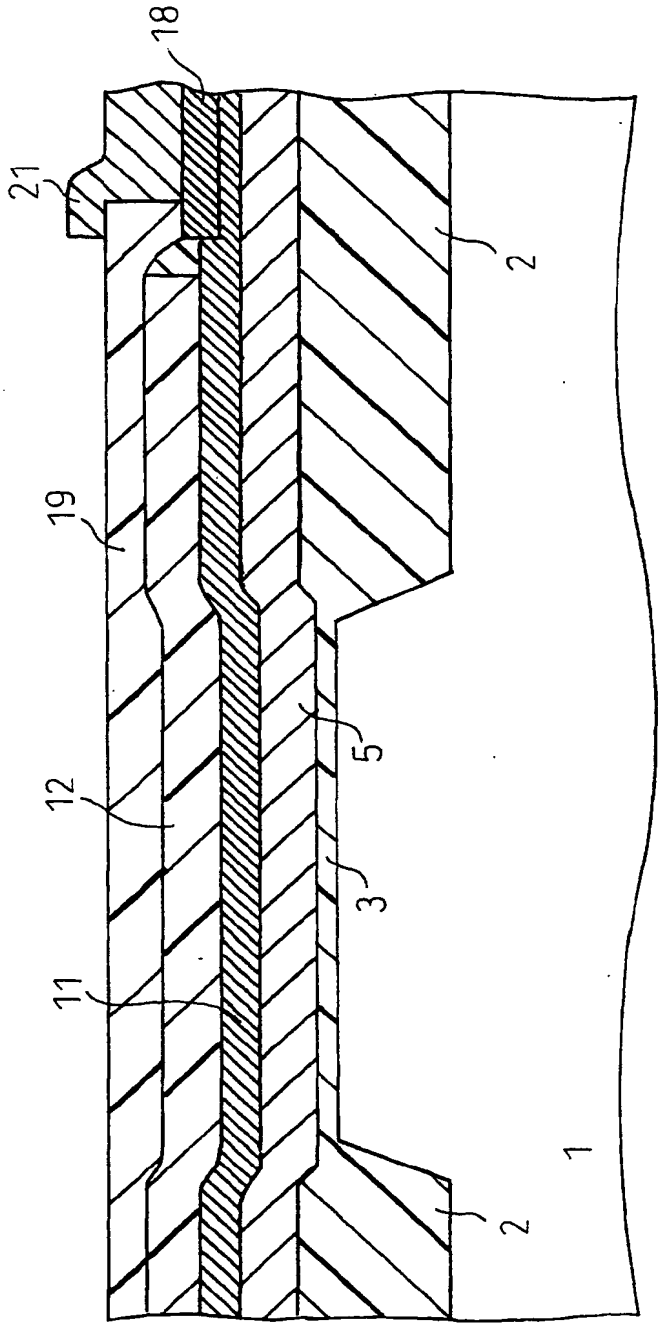


FIG. 10a2

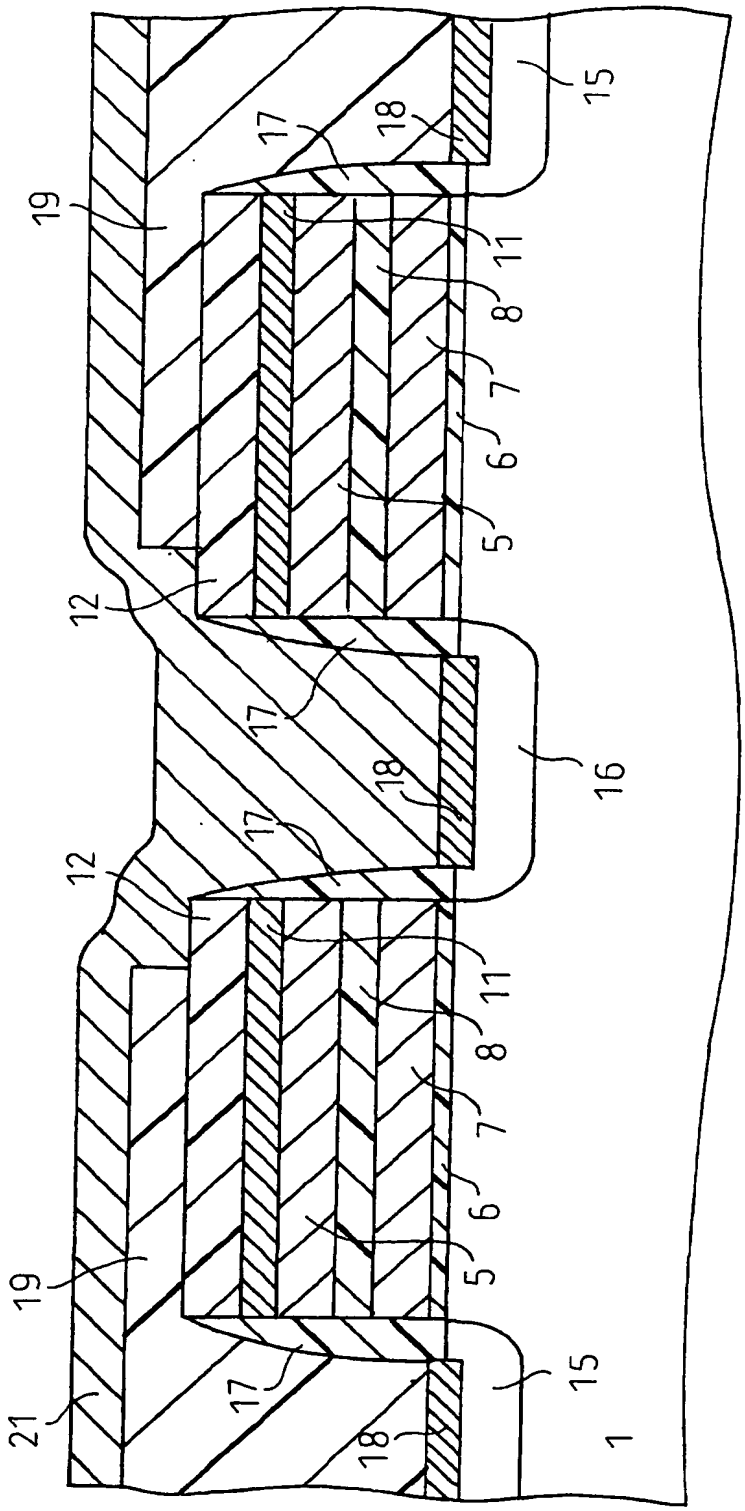


FIG. 10b

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EUROPEAN SEARCH REPORT

Application Number
EP 00 20 1716

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The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	31 October 2000	Albrecht, C

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